98 P2729

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

B1

(11) Publication number : **0 601 819 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93309776.8**

(51) Int. Cl.^{5} : **H04N 5/45**

(22) Date of filing : **06.12.93**

(30) Priority : **09.12.92 JP 329090/92**

(43) Date of publication of application :
15.06.94 Bulletin 94/24

(84) Designated Contracting States :
DE FR GB IT

(71) Applicant : **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
1006, Oaza Kadoma
Kadoma-shi, Osaka-fu, 571 (JP)

(72) Inventor : **Nakanishi, Masahiro**
Sanpurejio N202,
1032-1, Aotocho
Midori-ku, Yokohama-shi (JP)

(74) Representative : **Votier, Sidney David**
CARPMAELS & RANSFORD
43, Bloomsbury Square
London WC1A 2RA (GB)

(54) Image compression apparatus.

(57) A decoder (3) determines an averaging method in response to a compression ratio, and commands an adder circuit (22) and a shift register (25) so that an output of an A/D converter (1) is averaged. A clock decimation circuit (4) decimates a clock in response to a compression ratio, and a write unit (5) writes an averaged output of the shift register (25) in a memory (6) in response to a remaining clock. Data read out from the memory (6) by a read unit (7) is converted by a D/A converter (8) into an analog signal.

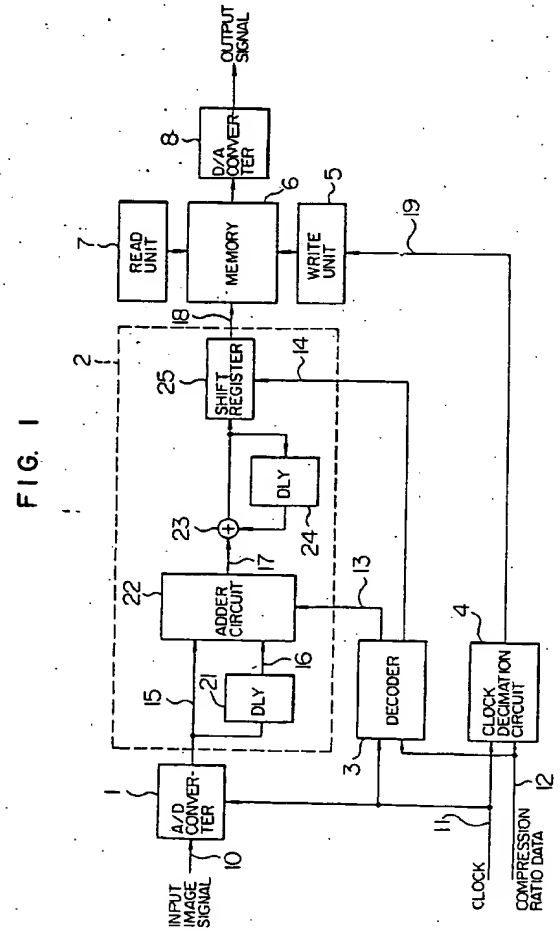


FIG. 1

EP 0 601 819 A1

BACKGROUND OF THE INVENTION

The present invention relates to an image compression apparatus for use in a video special effect apparatus of a television receiver or the like.

It is customary that, when a television picture is compressed in area and superimposed upon one portion of a picture screen of the television receiver, the number of scanning lines in the vertical direction is decimated and the number of pixels in the horizontal direction is decimated in response to a compression ratio, data that are not decimated are temporarily stored in a memory and then read out therefrom.

A conventional image compression apparatus of this kind includes a clock decimating circuit for decimating clocks in every vertical or horizontal direction in response to a compression ratio and uses an averaging method for averaging image data on the basis of a continuity of decimated clocks.

FIG. 3 of the accompanying drawings is a schematic block diagram showing a circuit arrangement of a conventional image compression apparatus. As shown in FIG. 3, this conventional image compression apparatus comprises an A/D (analog-to-digital) converter 31 for converting an input image signal into digital image data, a clock decimating circuit 33 for generating a decimation signal and a decimation clock on the basis of a write clock and compression ratio data, an averaging circuit 33 for averaging the image data in accordance with a remaining signal that is not decimated, a memory 35 for sequentially storing therein an output of the averaging circuit 32 in response to a remaining clock that is not decimated, a read circuit 36 for reading out the image data stored in the memory 35 and a D/A (digital-to-analog) converter 37 for converting the read-out image data into an analog signal. According to the conventional image compression apparatus thus arranged, a reduced image can be obtained with an arbitrary compression ratio.

SUMMARY OF THE INVENTION

However, the above-mentioned conventional image compression apparatus uses different averaging methods when an image is reduced with compression ratios of up to 1/2 in which decimated clocks are not continuous and when an image is reduced with compression ratios of less than 1/2 in which decimated clocks are continuous. Therefore, when an image compression ratio is changed successively, there is then the disadvantage that an image reduced with a compression ratio of less than 1/2 looks unnatural.

An object of the present invention is to provide an excellent image compression apparatus which can reduce an image with continuous compression ratios more naturally by using an averaging method that is not related to a continuity of clocks.

In order to attain the aforesaid object, an image compression apparatus according to an aspect of the present invention is comprised of an A/D conversion unit for converting an image signal into image data in synchronism with a write clock, a memory unit for temporarily storing therein the image data, a clock decimation unit for decimating a write clock in response to a compression ratio, a selection unit for determining an averaging method in response to a compression ratio, an averaging unit for averaging the image data by the averaging method determined by the selection unit, a write unit for outputting a write command in accordance with a remaining write clock that is not decimated, a read unit for reading out the image data from the memory unit, and a D/A conversion unit for converting the image data into an analog signal.

According to this image compression apparatus, when data representing a desired compression ratio is input thereto, a decimation clock corresponding to the desired compression ratio is generated, and an amount of image data to be averaged is determined on the basis of the compression ratio. Thus, decimated image data that are not written in the memory are averaged and then written in the memory so that an image can be reduced with an arbitrary compression ratio while the image can be prevented from becoming unnatural when reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram showing a circuit arrangement of an image compression apparatus according to an embodiment of the present invention;

FIG. 2 is a circuit diagram showing an example of an adder circuit used in the image compression apparatus shown in FIG. 1; and

FIG. 3 is a schematic block diagram showing a circuit arrangement of an image compression apparatus according to the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENT

An image compression apparatus according to an embodiment of the present invention will hereinafter be described with reference to the accompanying drawings.

FIG. 1 is a schematic block diagram showing a circuit arrangement of an image compression apparatus according to an embodiment of the present invention. FIG. 2 is a circuit diagram showing an example of an adder circuit used in the image compression apparatus shown in FIG. 1.

As shown in FIG. 1, an output 15 from an A/D converter 1 that digitizes an input image signal 10 is input to an averaging circuit 2 which averages image data. In the averaging circuit 2, a delay circuit (DLY) 21 is

supplied with the output from the A/D converter 1 and delays data by a predetermined period. An adder circuit 22 is adapted to average the output data of the A/D converter 1 and output data 16 of the delay circuit 21. Output data 17 from the adder circuit 22 is input to a full adder 23. Output data of a delay circuit (DLY) 24 that delays the output data of the full adder 23 by a predetermined period and the output data 17 of the adder circuit 22 are added by the full adder 23 and then input to a shift register 25. The averaging circuit 2 is arranged as described above.

There is shown a decoder (selection unit) 3 which determines and outputs an averaging method 13 of the adder circuit 22 and a shift number 14 of the shift register 25 on the basis of compression ratio data 12. There is shown a clock decimation circuit 4 which obtains clock decimation information from the compression ratio data to thereby decimate a clock 11. A write unit 5 that writes data on the basis of a remaining clock that is not decimated supplies a write command to a memory 6 which temporarily stores therein image data. A read unit 7 reads out image data from the memory 6, and a D/A converter 8 converts the image data thus read out from the memory 6 into an analog signal.

Operation of the image compression apparatus thus arranged will be described below.

When the compression ratio data 12 is input to the image compression apparatus of the present invention, the decoder 3 separates the input compression ratio data into compression ratio data representing compression ratios of 1/1 to 1/2 and compression ratio data representing compression ratios of $1/2^n$ (n = 0, 1, 2, ...) the products of which become the compression ratio data 12. When the compression ratio data 12 represents a compression ratio of 3/8, for example, $3/8 = (6/8) \times (1/2) = (3/4) \times (1/2)$. Thus, the decoder 3 outputs the averaging method 13 of the adder circuit 22 corresponding to the compression ratios of 1/1 to 1/2 and the shift number (n) 14 of the shift register 25 for reducing an image with the compression ratios of $1/2^n$.

As shown in FIG. 2, the adder circuit 22 is comprised of a switch 22a which is changed over by the averaging method 13, and full adders 22b, 22c and 22d to thereby average the image data digitized by the A/D converter 1 and the data 16 which results from delaying the image data 15 by the predetermined period by the delay circuit (DLY) 21. Referring back to FIG. 1, the averaged data 17 is added to the data from the delay circuit (DLY) 24 n times by the full adder 23, and the added result from the full adder 23 is rightwardly shifted by n bits by the shift register 25, for being output as an averaged output 18 thereby.

As described above, according to the embodiment of the present invention, any compression ratio data are expressed as (compression ratios of 1/1 to 1/2) × (compression ratio of $1/2^n$) and the averaging processing corresponding to such compression ratio data is effected so that a natural and continuous reduced image can be obtained.

The adder circuit 22 shown in FIG. 2 can effect the compression of 1/1 to 1/2 with a higher accuracy if the adder circuit 22 is modified in such a way as to further add switches and full adders or the like thereto.

As set forth, according to the present invention, it is possible to realize an excellent image compression apparatus which can reduce an image with continuous compression ratios while a reduced image can be prevented from becoming unnatural when displayed. In other words, image data of a television video signal can be reduced with continuous compression ratios by the simplified circuit arrangement while a reduced image can be prevented from becoming unnatural when displayed.

Claims

1. An image compression apparatus comprising:

A/D converting means (1) for converting an image signal into image data in synchronism with a write clock;

memory means (6) for temporarily storing therein said image data;

clock decimation means (4) for decimating said write clock in response to a compression ratio;

selecting means (3) for determining an averaging method in response to a compression ratio;

averaging means (2) for averaging image data by the averaging method determined by said selecting means (3);

write means (5) for outputting a write command to said memory means (6) in accordance with a remaining write clock that is not decimated;

read means (7) for reading out said image data from said memory means (6); and

D/A converting means (8) for converting said read-out image data into an analog signal.

FIG. 1

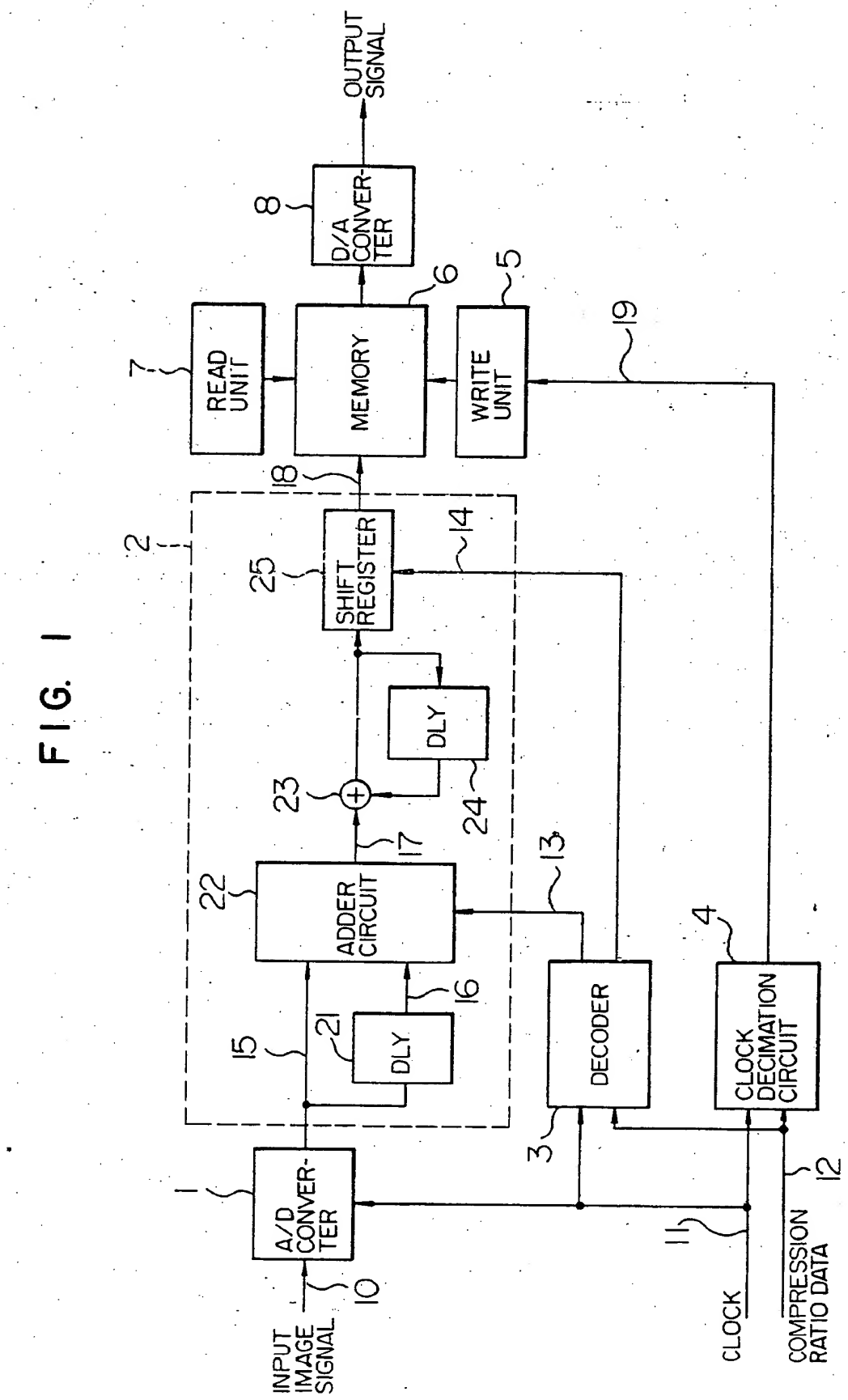

OUTPUT SIGNAL
8
D/A CONVERTER
6
5
7
READ UNIT
MEMORY
WRITE UNIT
19
18
2
25
SHIFT REGISTER
14
DLY
23
24
17
22
ADDER CIRCUIT
13
4
16
15
21
DLY
DECODER
CLOCK DECIMATION CIRCUIT
3
12
1
A/D CONVERTER
11
10
INPUT IMAGE SIGNAL
CLOCK
COMPRESSION RATIO DATA

FIG. 2

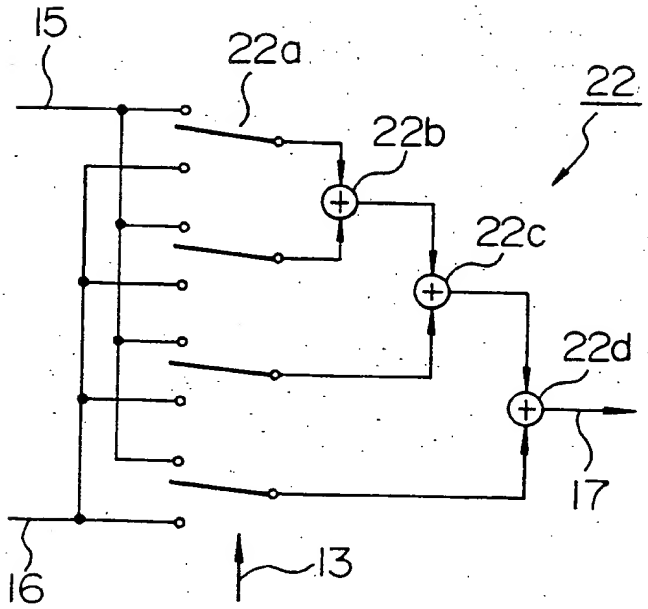
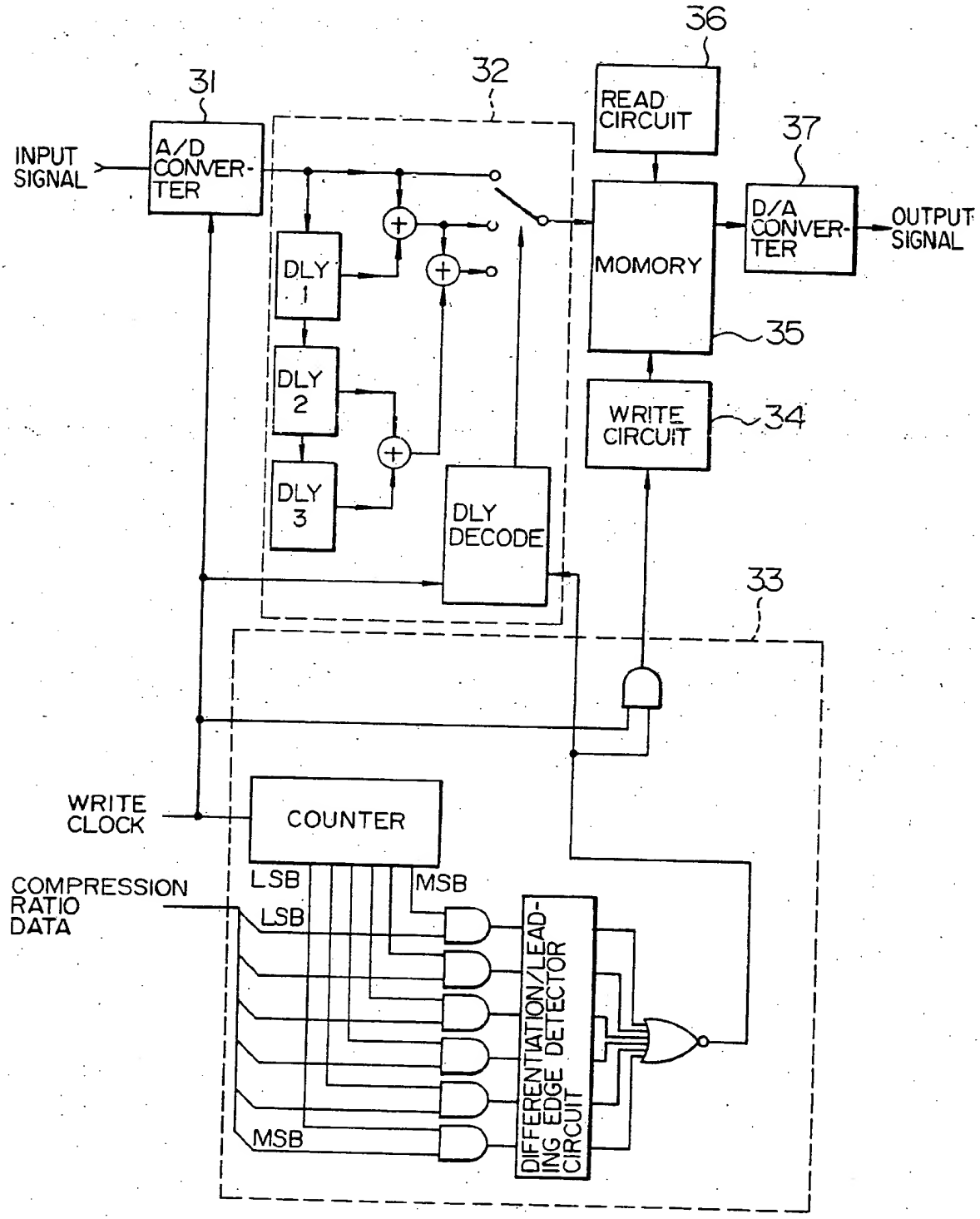


FIG. 3 PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 9776

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	EP-A-0 438 782 (NEC CORPORATION) * column 4, line 3 - column 7, line 36; figures 3,5 * -----	1	H04N5/45
			TECHNICAL FIELDS SEARCHED (Int.Cl.5) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	21 March 1994	Dudley, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)